OIPE JC99
FEB 20 2004
PATENT & TRADEMARK OFFICE

FIG. 1A

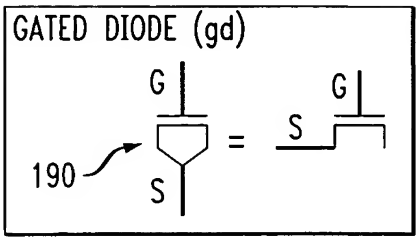

FIG. 1B

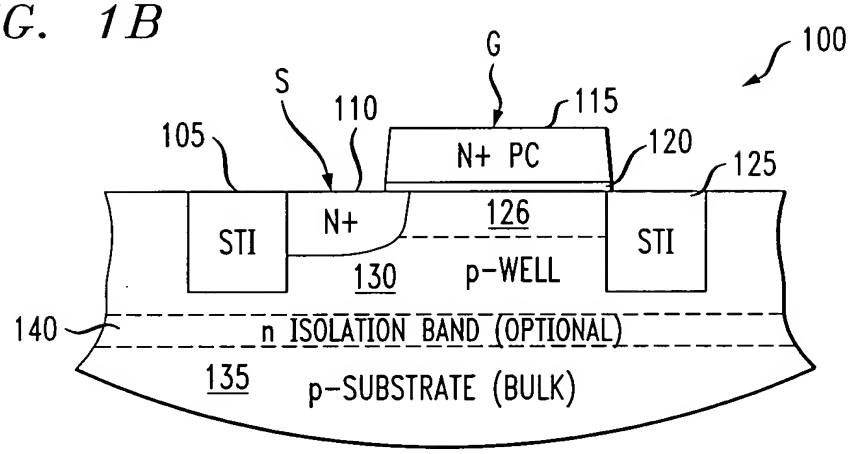

FIG. 1C

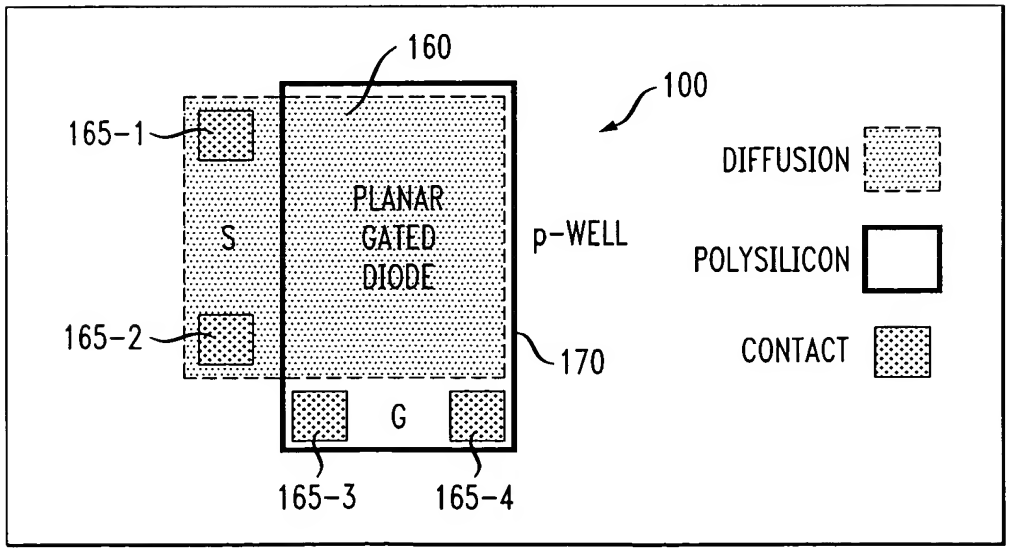

FIG. 2A

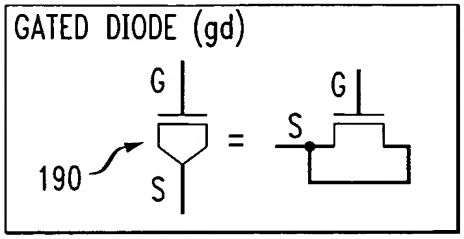

FIG. 2B

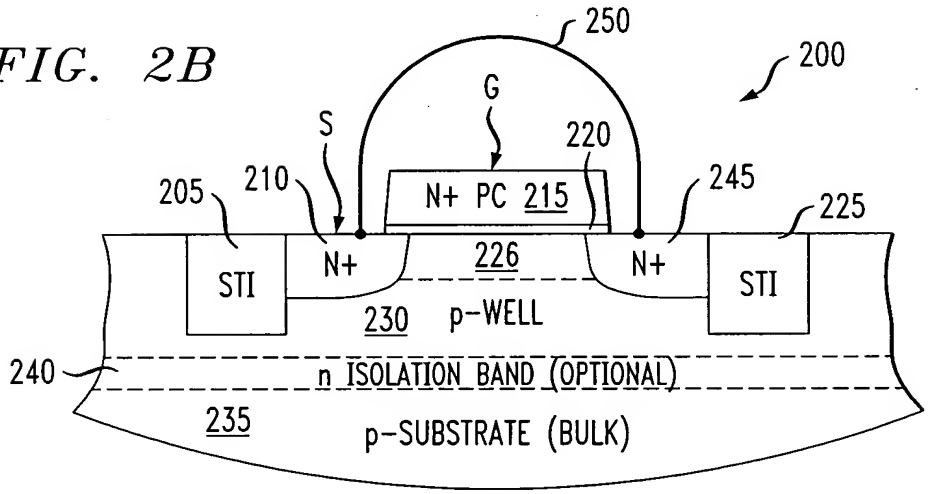

FIG. 2C

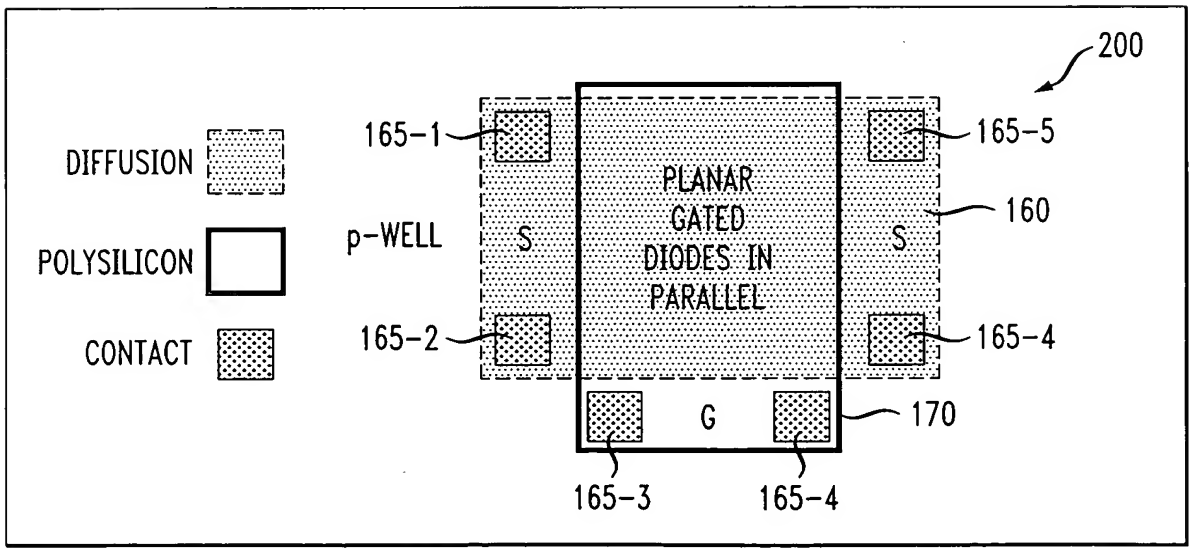

FIG. 3A

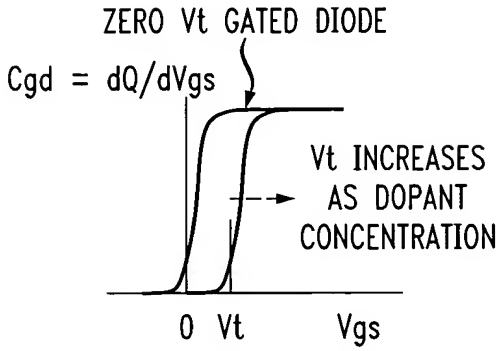

FIG. 3B

GATED DIODE CAPACITANCE vs GATE-TO-SOURCE VOLTAGE (Vgs)
EACH CURVE REPRESENTS A DIFFERENT GATED DIODE GATE SIZE.
THRESHOLD VOLTAGE = 0.2 V

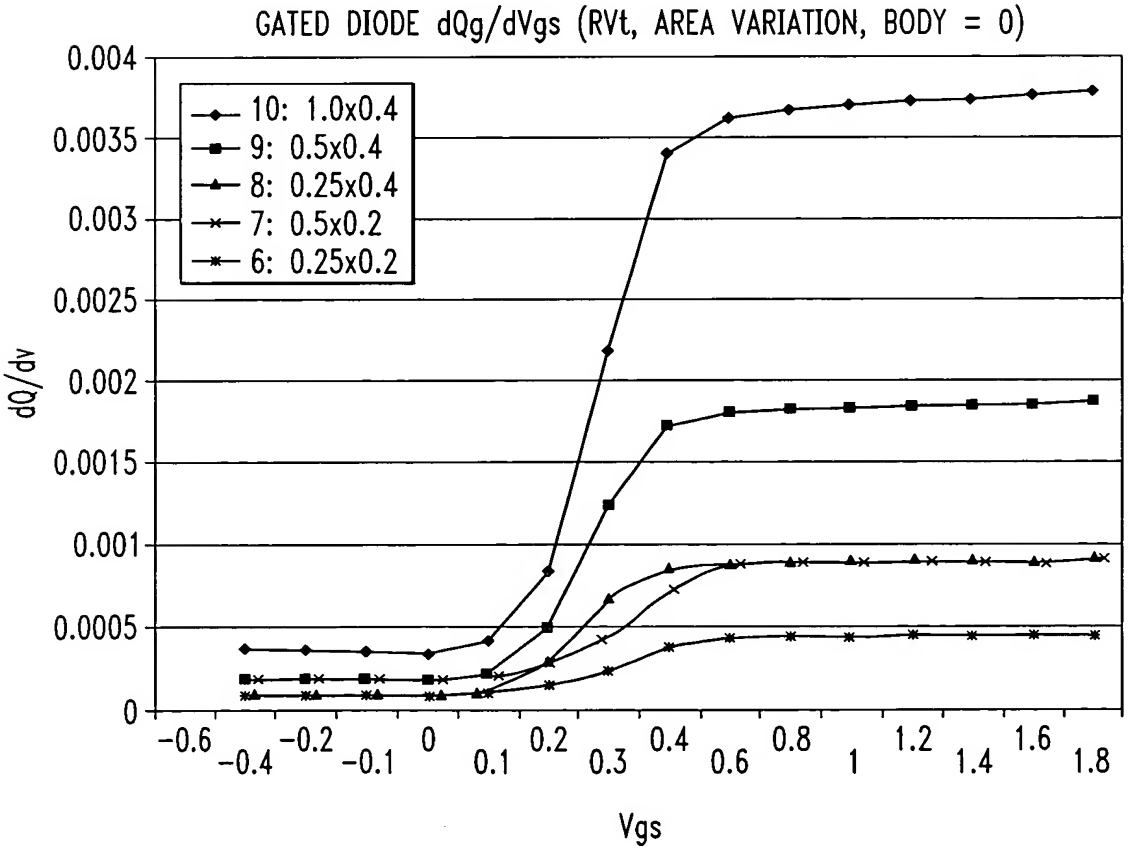

FIG. 4A

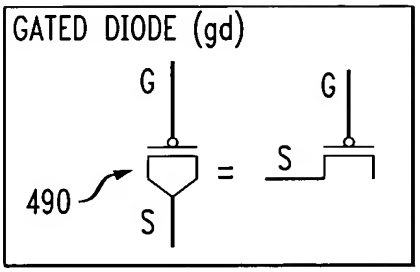
GATED DIODE (gd)
G
G
490
S
=
S

FIG. 4B

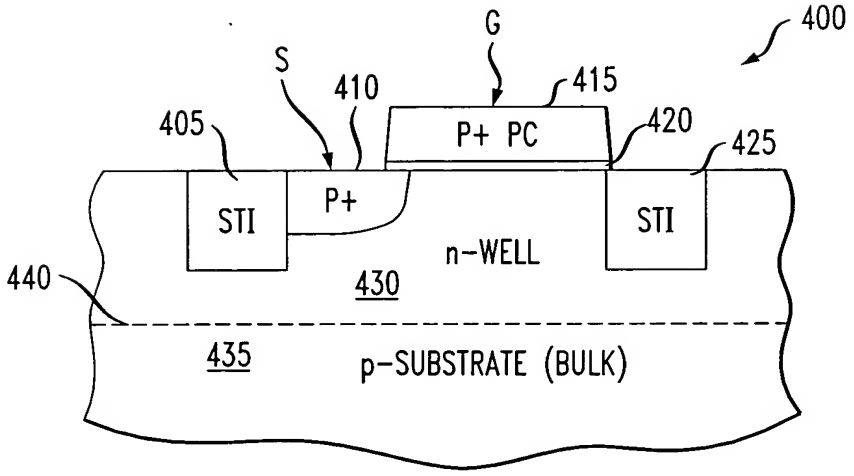
400
G
S
410
415
405
P+ PC
420
425
STI
P+
STI
n-WELL
440
430
435
p-SUBSTRATE (BULK)

FIG. 5A

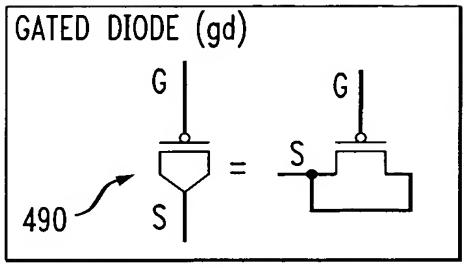
GATED DIODE (gd)
G
S
490
=
G
S

FIG. 5B

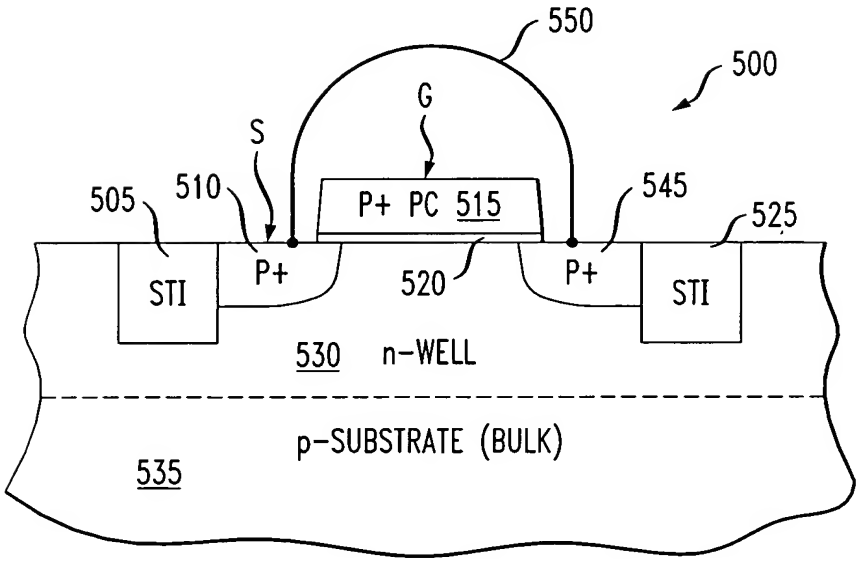
550
500
G
S
505
510
P+ PC 515
545
525
STI
P+
520
P+
STI
530 n-WELL
p-SUBSTRATE (BULK)
535

FIG. 6

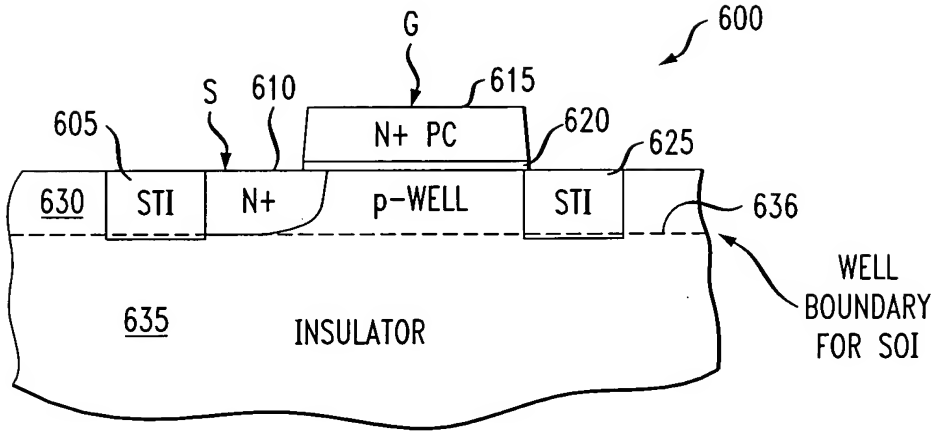
600
G
S
610
615
605
N+ PC
620
625
630
STI
N+
p-WELL
STI
636
WELL
BOUNDARY
FOR SOI
635
INSULATOR

FIG. 7

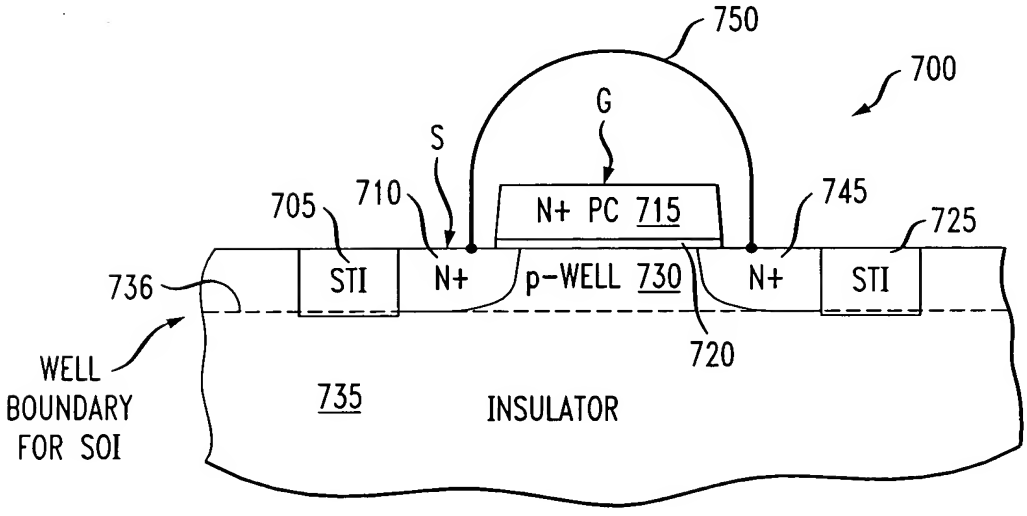
750
700
G
S
705
710
N+ PC 715
745
725
736
STI
N+
p-WELL 730
N+
STI
720
WELL
BOUNDARY
FOR SOI
735
INSULATOR

FIG. 8

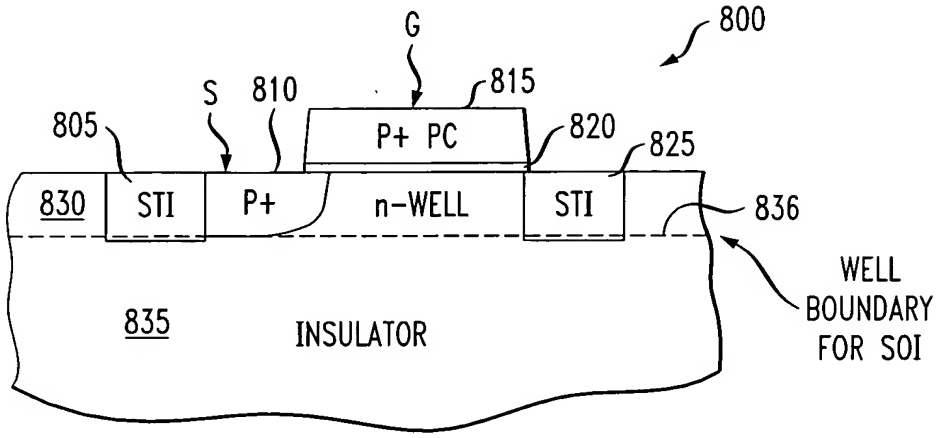

FIG. 9

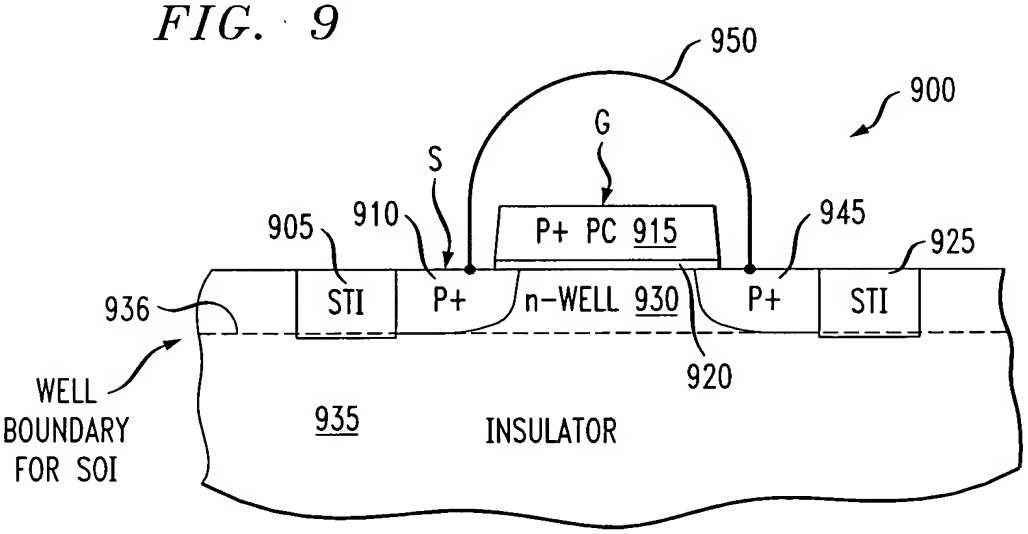

FIG. 10

LINEAR CAPACITOR
GAIN = dVout/dVin = 1

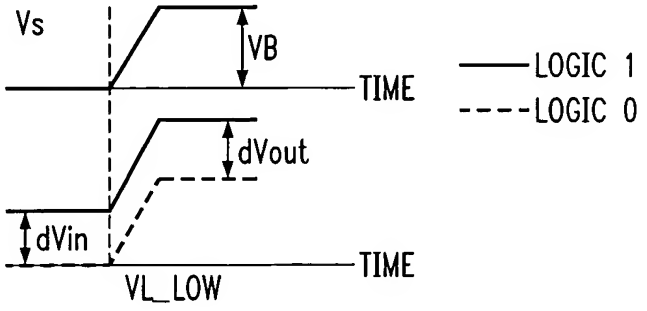

FIG. 11A

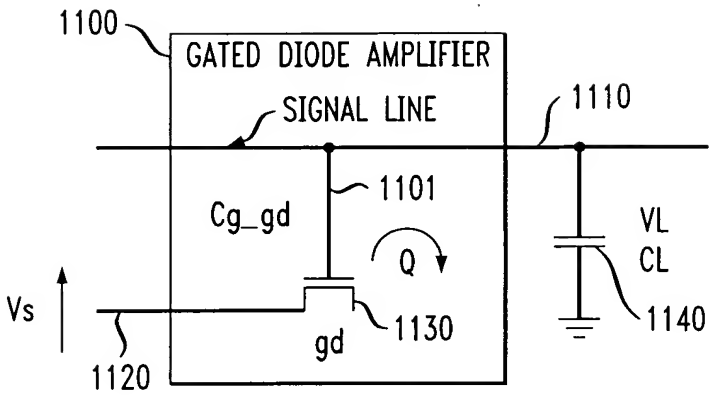

FIG. 11B

GATED DIODE AMPLIFIER REPRESENTATIVE CIRCUIT

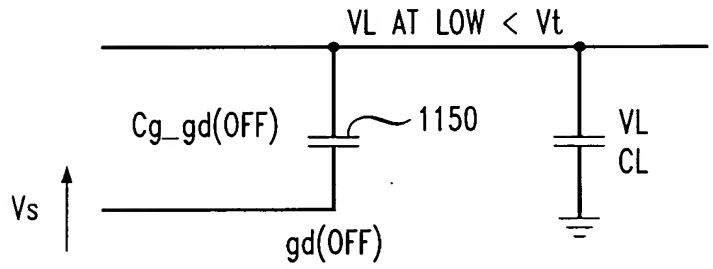

FIG. 11C

GATED DIODE AMPLIFIER REPRESENTATIVE CIRCUIT

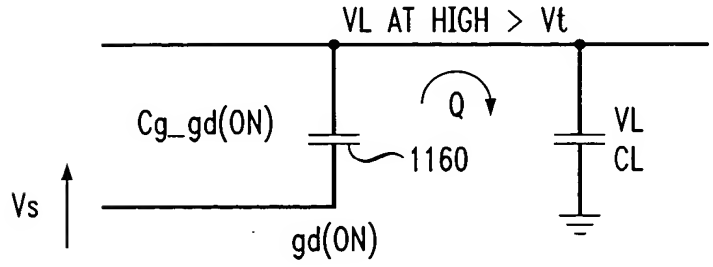

FIG. 12A

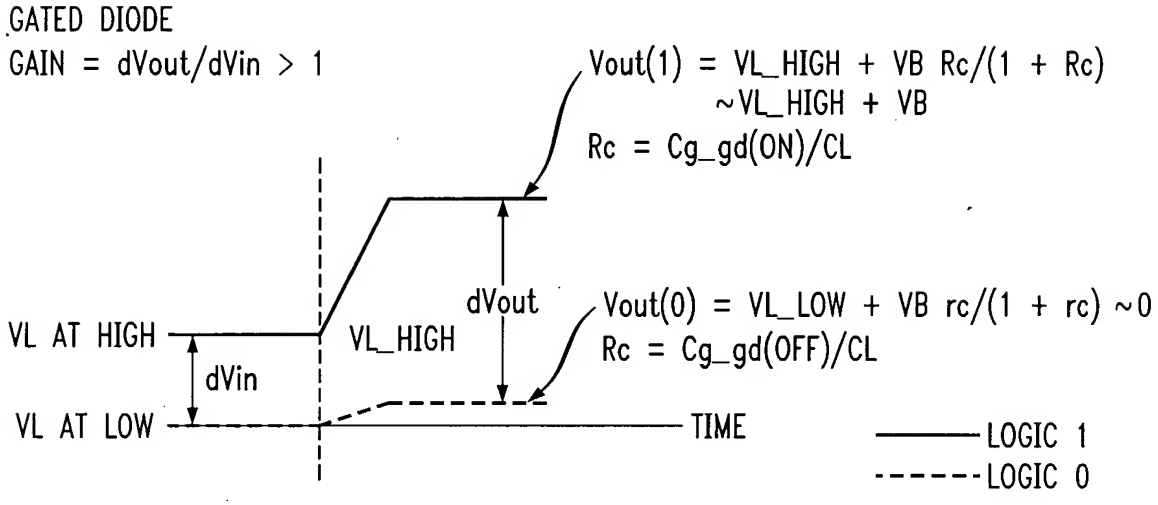

FIG. 12B

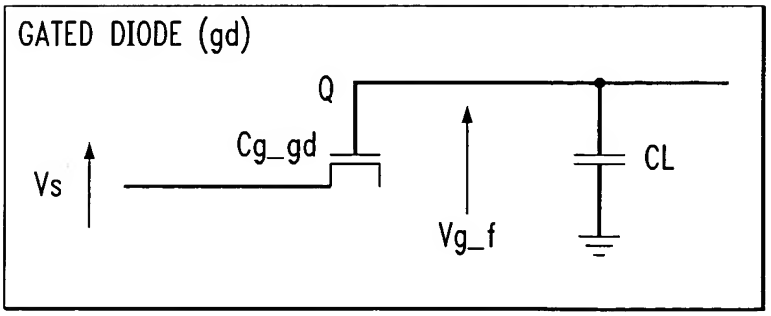

FIG. 12C

$Rc = Cg_gd/CL$
$GAIN = Vg_f/Vg_i$

$GAIN = 1 + Rc - (Vt_gd/Vg_i)\ Rc \sim 1 + Rc$ COMPLETE CHARGE TRANSFER (FOR SMALL Rc)
$GAIN = (1 + Vs/Vg_i)\ Rc/(1 + Rc)$ CONSTRAINED CHARGE TRANSFER (LARGE Rc)

$Vg_i = 0.4$ V, $Vt_gd = 0$

EXEMPLARY OPERATING POINT

Cg_gd/Cg_rg	0.01	0.1	1	2	5	10	100	
$1 + Rc$	1.01	1.1	2	3	6	11	101	
$Rc/(1 + Rc)$	0.01	0.09	0.5	0.67	0.83	0.91	0.99	
$(1+Vs/Vg_i)Rc/(1+Rc)$	0.035	0.32	1.75	2.35	2.91	3.19	3.47	$Vs/Vg = 2.5$
$(1+Vs/Vg_i)Rc/(1+Rc)$	0.04	0.36	2.00	2.68	3.32	3.64	3.96	$Vs/Vg = 3$
GAIN	1.01	1.1	2	2.68	3.32	3.64	3.96	$Vs/Vg = 3$
CHARGE TRANSFER	←--- COMPLETE ---→			←---- CONSTRAINED ----→				

FIG. 12D

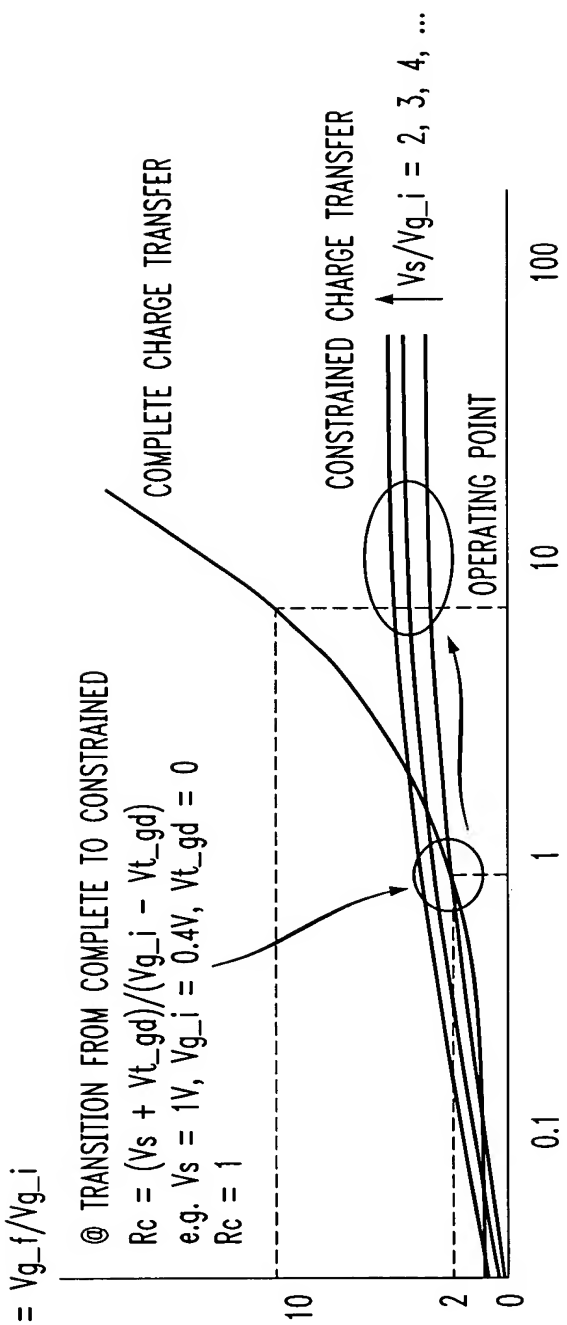
GAIN = Vg_f/Vg_i
@ TRANSITION FROM COMPLETE TO CONSTRAINED
Rc = (Vs + Vt_gd)/(Vg_i - Vt_gd)
e.g. Vs = 1V, Vg_i = 0.4V, Vt_gd = 0
Rc = 1
COMPLETE CHARGE TRANSFER
CONSTRAINED CHARGE TRANSFER
Vs/Vg_i = 2, 3, 4, ...
OPERATING POINT
10
2
0
0.1
1
10
100
Rc = Cg_gd/CL

FIG. 13

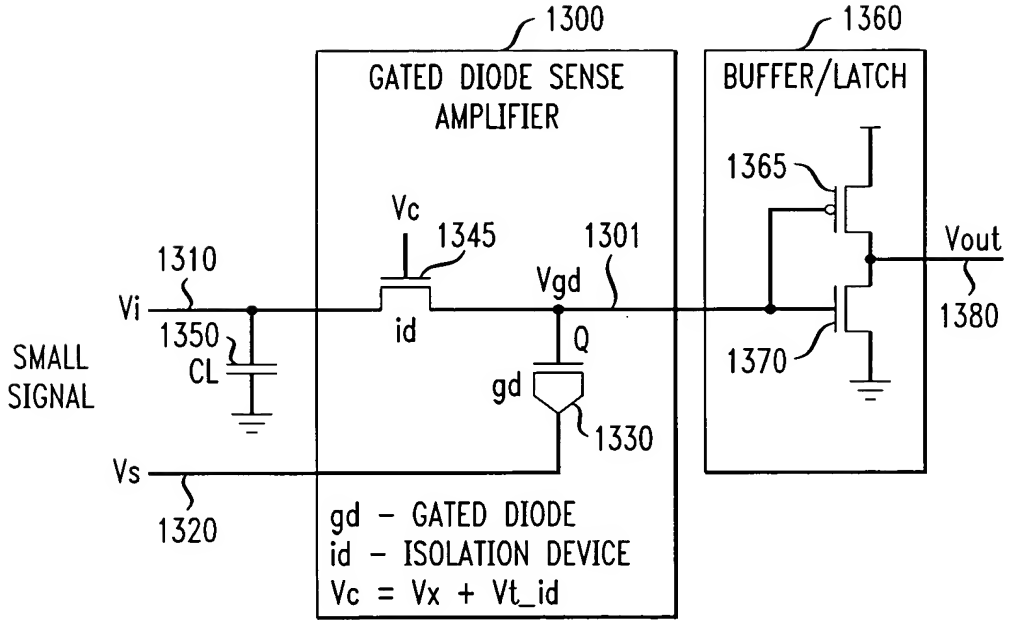
1300
GATED DIODE SENSE AMPLIFIER
1360
BUFFER/LATCH
1365
Vc
1345
1301
Vout
1310
Vi
Vgd
1350
CL
id
Q
1380
SMALL SIGNAL
1370
gd
1330
Vs
1320
gd - GATED DIODE
id - ISOLATION DEVICE
Vc = Vx + Vt_id

FIG. 14

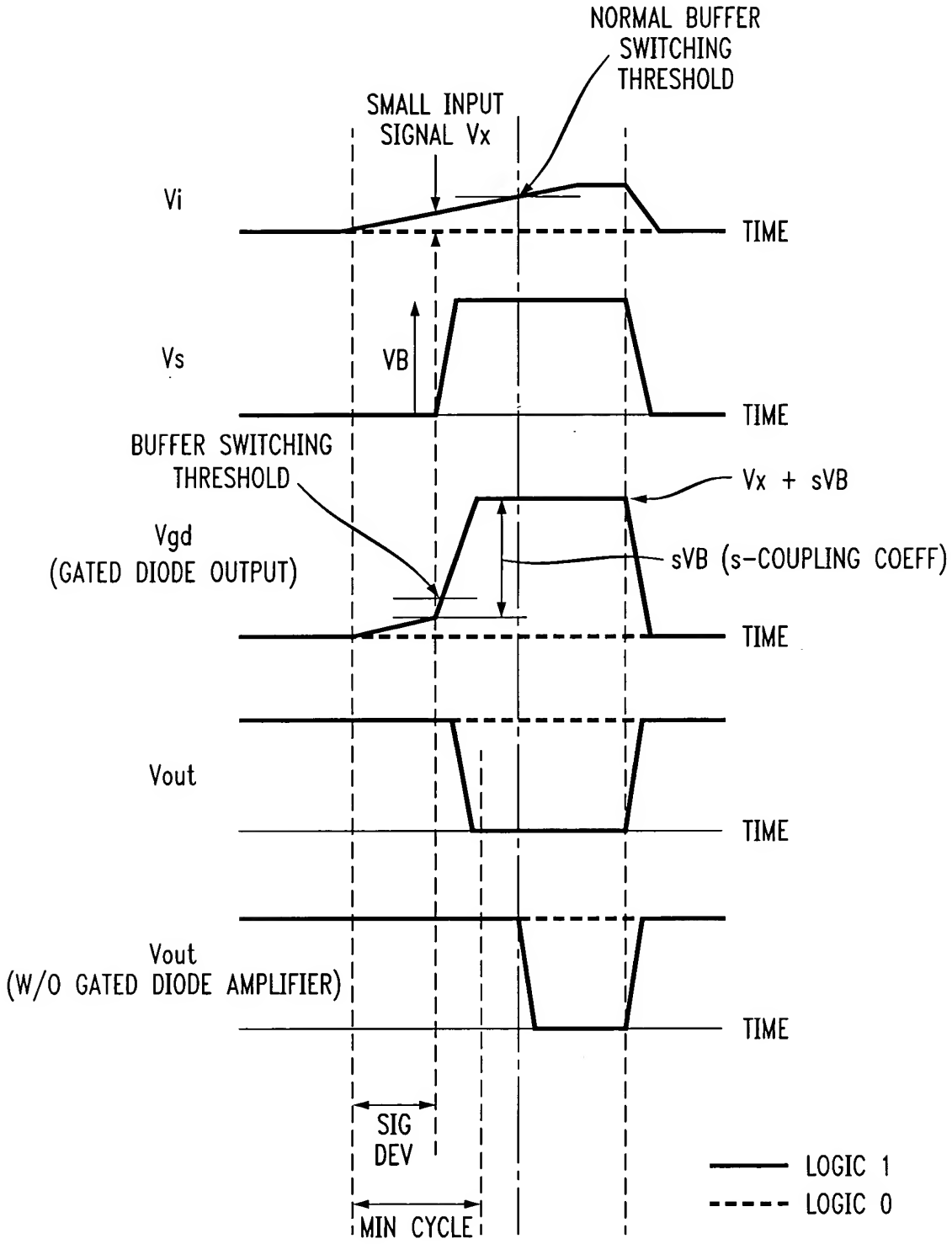
NORMAL BUFFER SWITCHING THRESHOLD
SMALL INPUT SIGNAL Vx
Vi
TIME
Vs
VB
TIME
BUFFER SWITCHING THRESHOLD
Vx + sVB
Vgd
(GATED DIODE OUTPUT)
sVB (s-COUPLING COEFF)
TIME
Vout
TIME
Vout
(W/O GATED DIODE AMPLIFIER)
TIME
SIG DEV
MIN CYCLE
LOGIC 1
LOGIC 0

FIG. 15

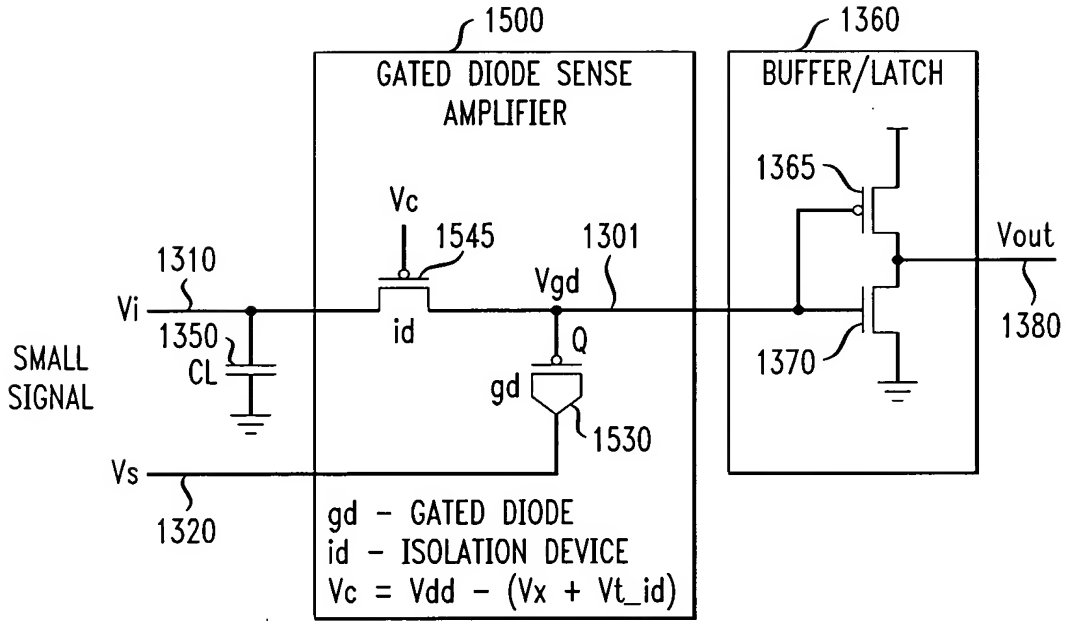
1500
GATED DIODE SENSE AMPLIFIER
1360
BUFFER/LATCH
1365
Vc
1545
1301
Vout
1310
Vi
Vgd
1350
CL
id
Q
1380
SMALL SIGNAL
1370
gd
1530
Vs
1320
gd - GATED DIODE
id - ISOLATION DEVICE
Vc = Vdd - (Vx + Vt_id)

FIG. 16

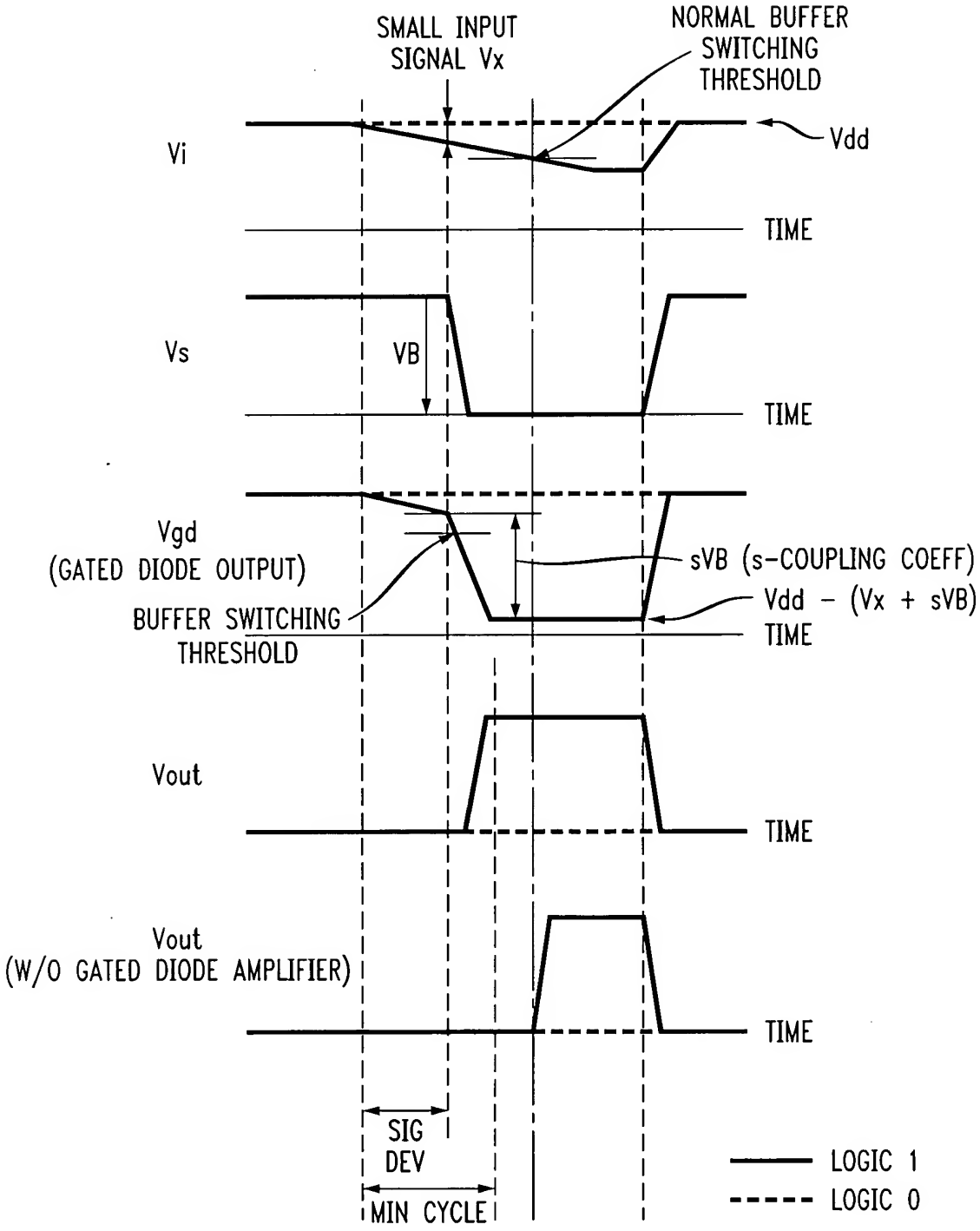
SMALL INPUT SIGNAL Vx
NORMAL BUFFER SWITCHING THRESHOLD
Vi
Vdd
TIME
Vs
VB
TIME
Vgd
(GATED DIODE OUTPUT)
sVB (s-COUPLING COEFF)
Vdd - (Vx + sVB)
BUFFER SWITCHING THRESHOLD
TIME
Vout
TIME
Vout
(W/O GATED DIODE AMPLIFIER)
TIME
SIG DEV
MIN CYCLE
LOGIC 1
LOGIC 0

FIG. 17

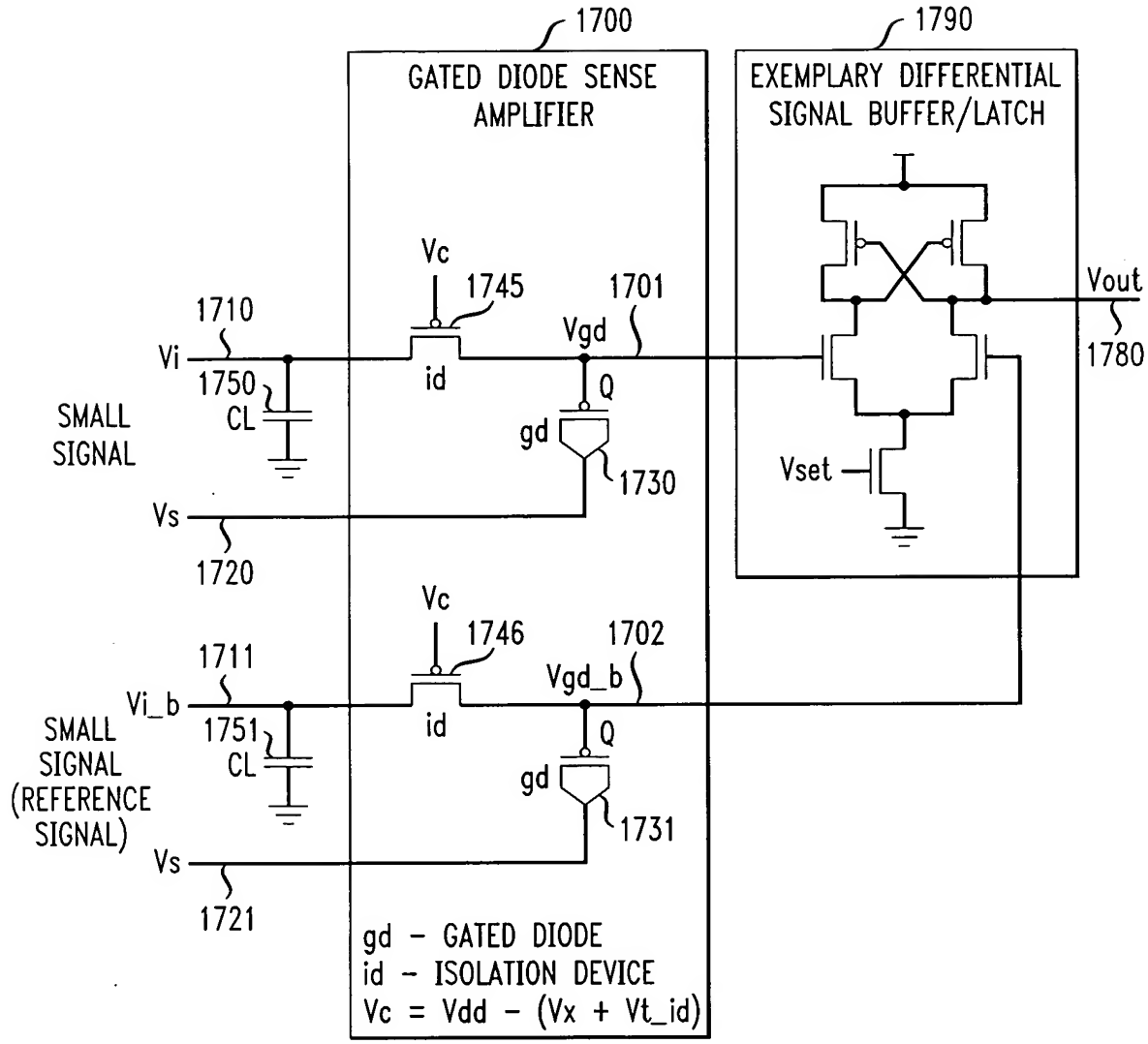
1700
GATED DIODE SENSE AMPLIFIER
1790
EXEMPLARY DIFFERENTIAL SIGNAL BUFFER/LATCH
Vc
1745
1701
Vgd
Vout
1780
1710
Vi
1750
CL
SMALL SIGNAL
id
Q
gd
1730
Vset
Vs
1720
Vc
1746
1702
Vgd_b
1711
Vi_b
1751
CL
SMALL SIGNAL (REFERENCE SIGNAL)
id
Q
gd
1731
Vs
1721
gd - GATED DIODE
id - ISOLATION DEVICE
Vc = Vdd - (Vx + Vt_id)

FIG. 18

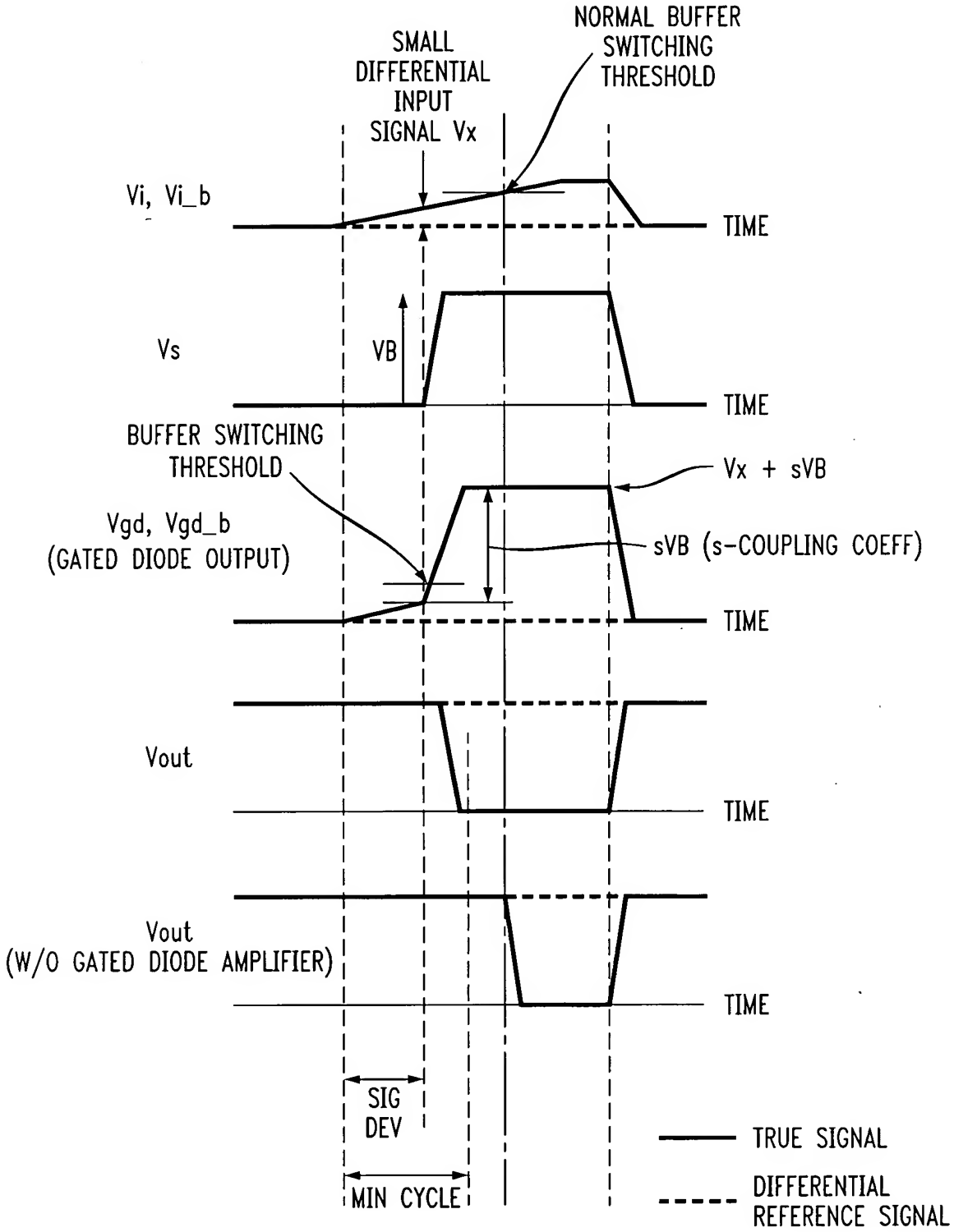
NORMAL BUFFER SWITCHING THRESHOLD
SMALL DIFFERENTIAL INPUT SIGNAL Vx
Vi, Vi_b
TIME
Vs
VB
TIME
BUFFER SWITCHING THRESHOLD
Vx + sVB
Vgd, Vgd_b (GATED DIODE OUTPUT)
sVB (s-COUPLING COEFF)
TIME
Vout
TIME
Vout (W/O GATED DIODE AMPLIFIER)
TIME
SIG DEV
MIN CYCLE
TRUE SIGNAL
DIFFERENTIAL REFERENCE SIGNAL

FIG. 19A

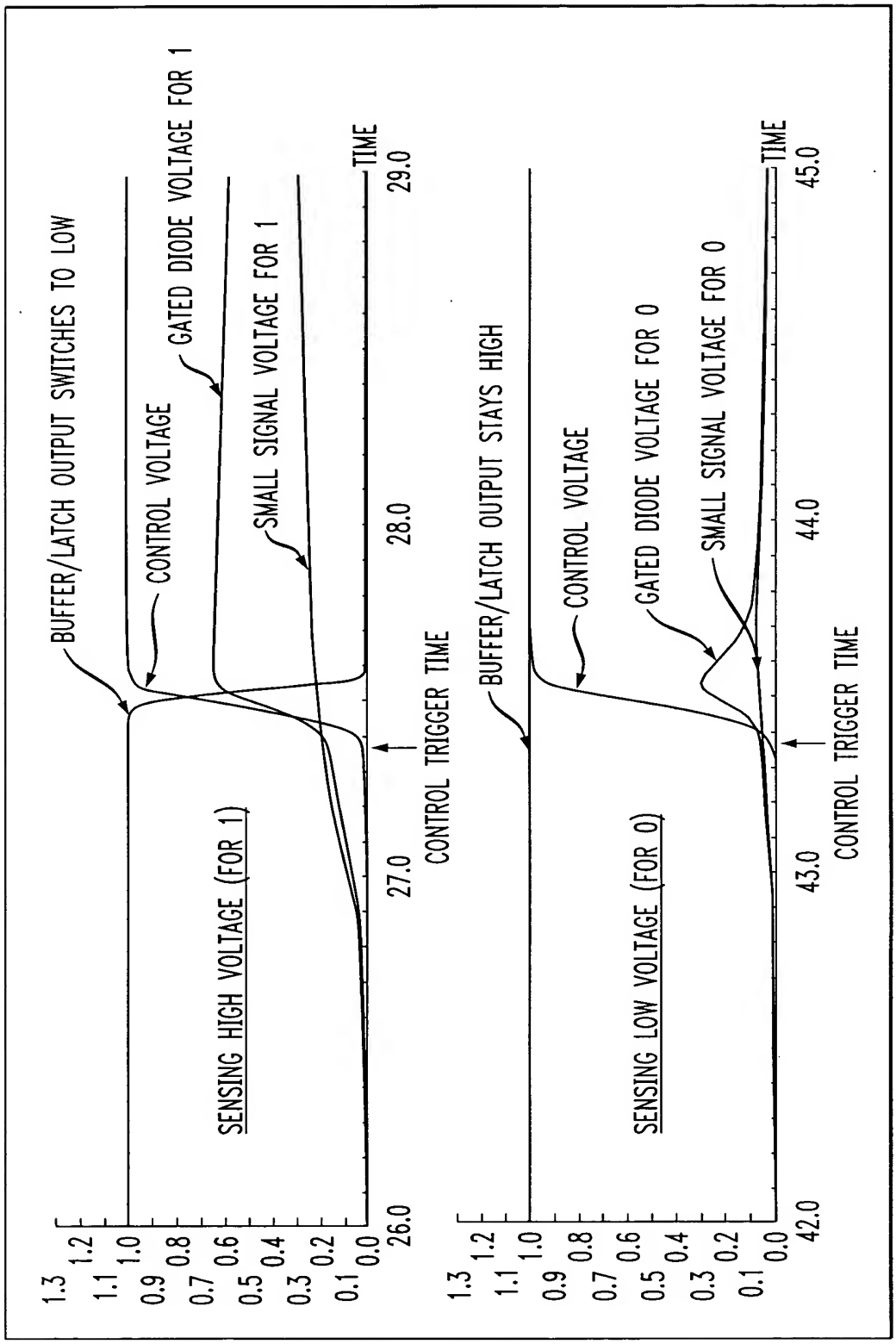
BUFFER/LATCH OUTPUT SWITCHES TO LOW
CONTROL VOLTAGE
GATED DIODE VOLTAGE FOR 1
SMALL SIGNAL VOLTAGE FOR 1
SENSING HIGH VOLTAGE (FOR 1)
TIME
26.0
27.0
28.0
29.0
CONTROL TRIGGER TIME
BUFFER/LATCH OUTPUT STAYS HIGH
CONTROL VOLTAGE
GATED DIODE VOLTAGE FOR 0
SMALL SIGNAL VOLTAGE FOR 0
SENSING LOW VOLTAGE (FOR 0)
TIME
42.0
43.0
44.0
45.0
CONTROL TRIGGER TIME
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0

FIG. 19B

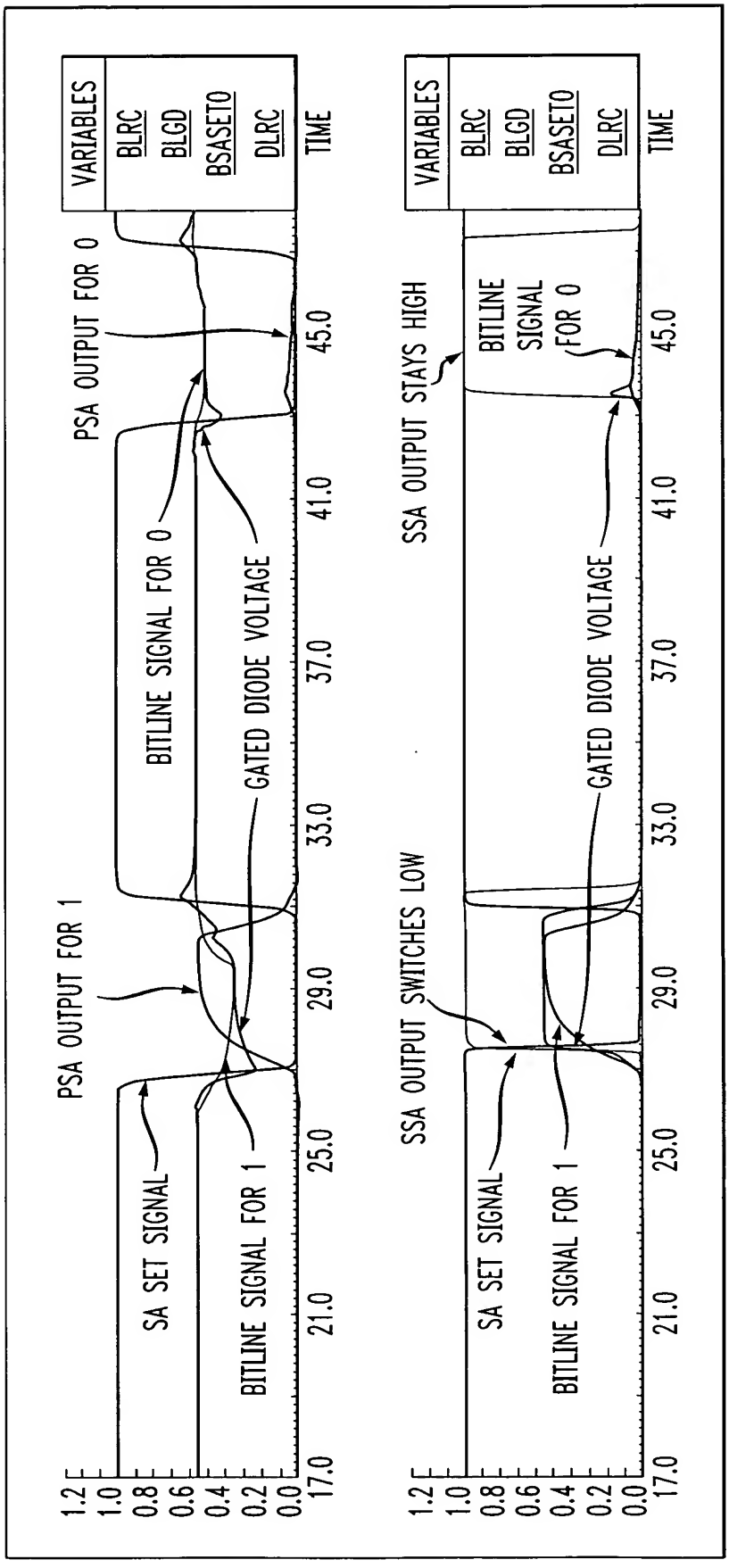
VARIABLES
BLRC
BLGD
BSASETO
DLRC
TIME
PSA OUTPUT FOR 0
BITLINE SIGNAL FOR 0
GATED DIODE VOLTAGE
PSA OUTPUT FOR 1
SA SET SIGNAL
BITLINE SIGNAL FOR 1
SSA OUTPUT STAYS HIGH
SSA OUTPUT SWITCHES LOW
1.2
1.0
0.8
0.6
0.4
0.2
0.0
17.0
21.0
25.0
29.0
33.0
37.0
41.0
45.0

FIG. 20A

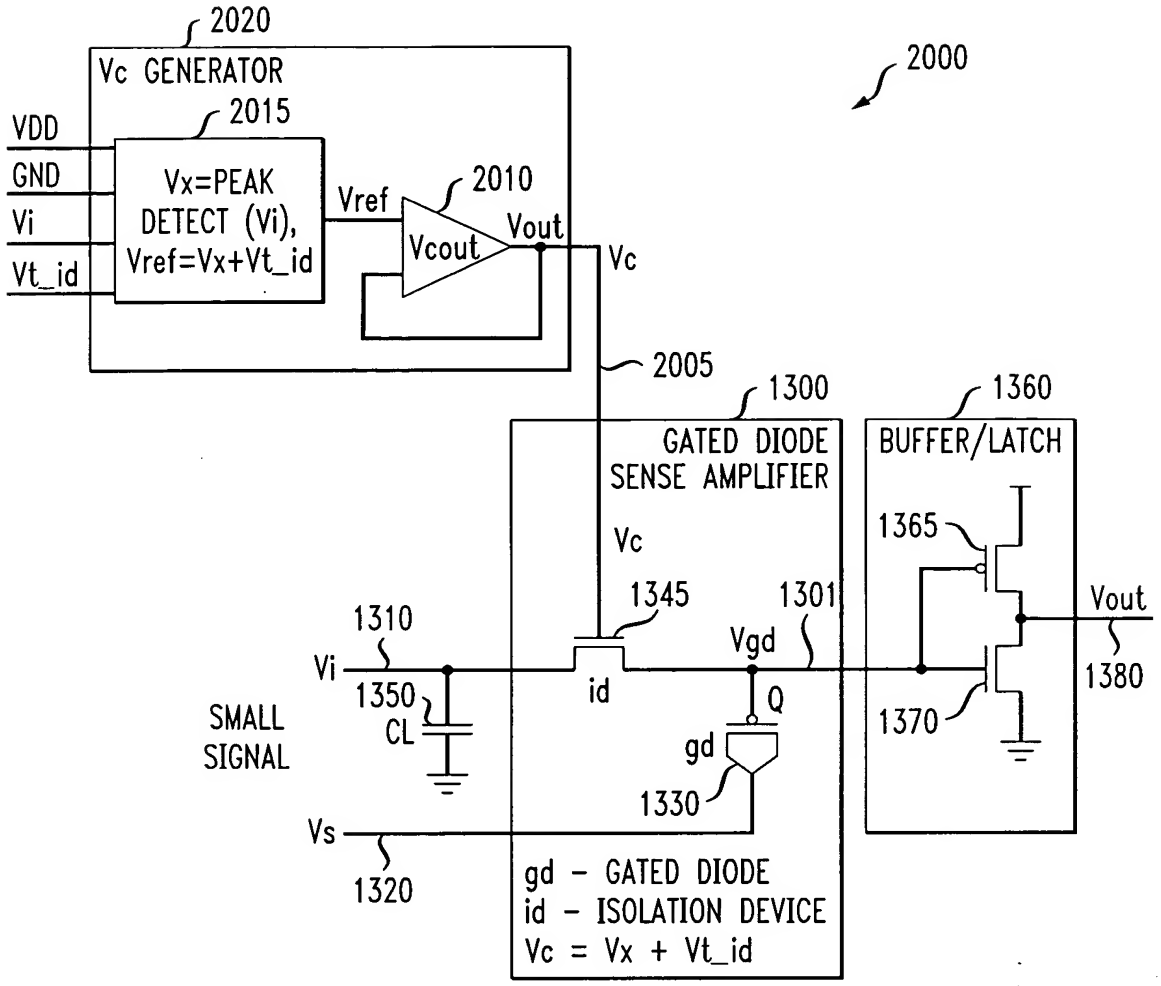
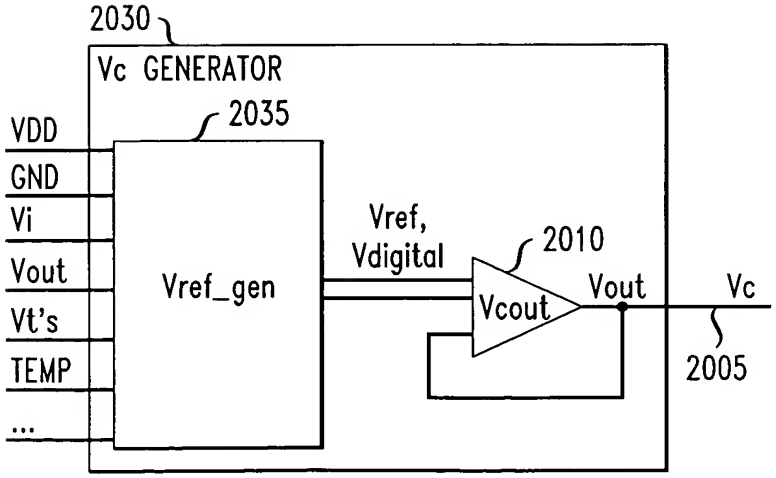
FIG. 20B